Russell Randolph

ASIC and FPGA Contractor
Portland, Oregon 503-327-1944

EXPERIENCE:

Engineering Contractor (for various companies) (1999 to present)

- Harmonic / Omneon Video Systems: SMPTE SDI video and ancillary data processing. Worked on multiple encoders and decoders in various formats (MPEG-2, DV, DnxHD (VC-3), Prores).
- Intel Probe FPGA design: Created synthesizable Verilog for most of the probe's FPGA and the validation platform's FPGA. Created Modelsim testbench, synthesized FPGA, and validated functionality in lab.
- C-Cor FPGA design: Wrote Verilog code for Ethernet packet parsing block. Created testbench for validating MPEG video traffic through the FPGA blocks. Helped with various microarchitecture design issues.
- Intel system bus visibility ASIC: Wrote unit level and full chip validation tests in Verilog. Created tools to split ASIC into two FPGAs for a software validation platform. Synthesized the FPGAs.
- Intel PCI Express validation ASIC: Developed VHDL unit level test bench. Wrote unit level and full chip tests that included PCI Express and i960 bus interfaces.
- Simutech FPGA based system simulation/validation platform: Developed Verilog test bench for validation of modules. Created system compilation environment for simulation, synthesis and place and route which supported multiple FPGA vendors and chips. Created system critical path and maximum frequency determination tool using multiple FPGA vendors' timing tools.
- nCUBE video server engineering: Performed simulations to create fault tolerant node cabling configurations. Wrote PCI-X and SDRAM DDR testbench models. Integrated testbench to Verilog using PLI interface. Developed targeted full chip ASIC tests. Reviewed system architecture proposals. Completed performance analysis and improvement suggestions (both software and hardware) for an OC-48 I/O card.
- Stexar Standard Cell Library: Created standard cell library, including LVS netlists and Verilog models. Reviewed layout. Studied noise and crosstalk issues.
- Translogic Technology ASIC cell library test chips: Tasks included creating the specification, Verilog model, testbench and tests, a Verilog to spice converter for LVS, layout of the chip, running DRC and LVS, interfacing with the foundry and packaging companies, and developing chip testing strategies.
- Expert for plaintiff in patent infringement case: Created tools and analyzed defendant's microprocessors to find infringing circuits. Filed many expert reports and witness statements. Deposed 3 times, testified in 2 jury trials, and gave a tutorial to the judge.

nCUBE (1990 to 1999)

- nCUBE4 video server: Developed system and ASIC architecture for video data flow. Wrote PCI bus event driver testbench in C. Created nHDL language and preprocessors to convert to ANSI C code or synthesizable Verilog. Owner of SDRAM controller (architecture, HDL, synthesis, tests).
- nCUBE3 massively parallel computer: Designed floating point unit including hardware add, subtract, multiply, divide and square root (architecture, RTL, logic, circuits, tests, debug). Created random and targeted floating point tester for both RTL and silicon. Wrote random and targeted instruction validation test tools for nCUBE3 RTL and silicon.

Intel Oregon Microprocessor Engineering (1984 to 1990)

- Worked on multiple 960 family microprocessors and support chips. Responsibilities included RTL simulator, logic, circuits, test writing, silicon debug, electromigration and ESD.

Signetics MOS Memory Group (1982 to 1984)

- Designed 2Kx16 CMOS SRAM, and debugged and characterized ROM and EPROM components.

SKILLS:

- Program in C, Awk, Perl, Unix shells (bash, tcsh) and Make.
- Extensive use of VHDL, Verilog, and Verilog's PLI interface.
- ASIC contractor, VLSI design, FPGA coding and synthesis, chip and block validation.
- Have used CAD tools from Synopsys, Cadence, Mentor Graphics, Altera and Xilinx.

EDUCATION:

- Bachelor's Degree in Physics, University of California, San Diego, 1982.